WHAT IS CLAIMED IS:

1. A semiconductor structure comprising:

a semiconductor substrate that includes a first semiconductor material and a second semiconductor material wherein the first semiconductor material has a lattice constant that is different from a lattice constant of the second material;

a first transistor formed in the semiconductor substrate, the first transistor having first source and drain regions formed in the substrate oppositely adjacent a first channel region, wherein a first gate dielectric overlies the first channel region and a first gate electrode overlies the first gate dielectric, and wherein the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material; and

a second transistor formed in the semiconductor substrate, having a conductivity type different than the first transistor, the second transistor having second source and drain regions in the substrate oppositely adjacent a second channel region, wherein a second gate dielectric covers the second channel region and a second gate electrode covers the second gate dielectric.

2. The structure of claim 1 wherein the first transistor is coupled to the second transistor to form an inverter.

3. The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of a NOR circuit.

4. The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of a NAND circuit.

5. The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of an XOR circuit.

6. The structure of claim 1 wherein the first and second gate dielectrics are formed from a high-k dielectric.

7. The structure of claim 1 wherein the first and second gate electrodes comprise a metal material.

8. The structure of claim 1 wherein the lattice constant of the second semiconductor material is larger than the lattice constant of the first semiconductor material.

9. The structure of claim 8 wherein the first transistor is a PMOS transistor.

10. The structure of claim 9 wherein the second semiconductor material comprises silicon (Si) and germanium (Ge).

11. The structure of claim 10 wherein the second semiconductor material comprises Silicon (Si), Germanium (Ge), and Carbon (C).

12. The structure of claim 10 wherein the concentration of Ge is greater than 10 percent.

13. The structure of claim 1 wherein the lattice constant of the second semiconductor material is smaller than the lattice constant of the first semiconductor material.

14. The structure of claim 13 wherein the first transistor is an NMOS transistor.

15. The structure of claim 14 wherein the second semiconductor material comprises silicon and carbon.

16. The structure of claim 15 wherein the second semiconductor material comprises silicon, germanium, and carbon.

17. The structure of claim 15 wherein the concentration of carbon is in the range of 0.01 percent to 0.04 percent.

18. The structure of claim 1 further comprising a third semiconductor material, wherein at least a portion of the second source and drain regions are formed in the third semiconductor material.

19. The structure of claim 18 wherein the lattice constant of the second semiconductor material is larger than lattice constant of the first semiconductor material and the lattice constant of the third material is smaller than the lattice constant of the first material.

20. The structure of claim 19 wherein the first transistor is a PMOS and the second transistor is an NMOS.

21. The structure of claim 19 wherein the third semiconductor material comprises silicon, germanium and carbon.

22. The structure of claim 1 wherein the first transistor comprises a PMOS transistor and the second transistor comprises an NMOS transistor and wherein the ratio of a width of the gate of

the PMOS transistor to a width of the gate of the NMOS transistor is approximately equal to the square root of a ratio of electron mobility to the hole mobility in the channel region.

23. The structure of claim 1 wherein the first transistor comprises a PMOS transistor and the second transistor comprises an NMOS transistor and wherein the ratio of a width of the gate of the PMOS transistor to a width of the gate of the NMOS transistor is approximately equal to the ratio of electron mobility to hole mobility in the channel region.

24. The structure of claim 1 wherein the first and second source and drain regions and the gate electrodes of the first and second transistors each include a silicided portion.

25. The structure of claim 1 wherein the distance between a junction between the first semiconductor material and the second semiconductor material and the gate dielectric edge is less than 700 angstroms.

26. An inverter comprising:

a transistor formed in the semiconductor substrate, the transistor having a source region and a drain region formed in a semiconductor substrate oppositely adjacent a channel region, wherein the channel is formed in a first semiconductor material and at least a portion of the source region and the drain region is formed in a second semiconductor material, the first semiconductor material being different than the second semiconductor material ;

a load element formed in the semiconductor substrate, the load element coupled between the drain region and a first supply voltage node; and

a second supply voltage node coupled to the source region.

27. The inverter of claim 26 wherein the load element comprises a resistor and the transistor comprises an NMOS transistor.

28. The inverter of claim 26 wherein the load element comprises a resistor and the transistor comprises a PMOS transistor.

29. The inverter of claim 26 wherein the load element comprises a transistor.

30. The inverter of claim 29 wherein the load element comprises a strained transistor.

31. The inverter of claim 26 wherein the transistor includes a gate dielectric overlying the channel region, the gate dielectric being formed from a high-k dielectric.

32. The inverter of claim 31 wherein the transistor includes a gate electrode overlying the gate dielectric, the gate electrode comprising a metal material.

33. The inverter of claim 26 wherein a lattice constant of the second semiconductor material is larger than a lattice constant of the first semiconductor material.

34. The inverter of claim 33 wherein the transistor is a PMOS transistor.

35. The inverter of claim 34 wherein the second semiconductor material comprises silicon (Si) and germanium (Ge).

36. The inverter of claim 35 wherein the concentration of Ge is greater than 10 percent.

37. The inverter of claim 26 wherein the lattice constant of the second semiconductor material is smaller than the lattice constant of the first semiconductor material.

38. The inverter of claim 37 wherein the transistor is an NMOS transistor.

39. The inverter of claim 38 wherein the second semiconductor material comprises silicon (Si), germanium (Ge), and carbon (C).

40. The inverter of claim 39 wherein the concentration of carbon is in the range of 0.01 percent to 0.04 percent.

41. The inverter of claim 26 wherein the first and second source and drain regions and the gate electrodes of the first and second transistors each include a silicided portion.

42. The inverter of claim 26 wherein the first semiconductor material consists essentially of silicon.

43. The inverter of claim 42 wherein the second semiconductor material comprises silicon and germanium.

44. The inverter of claim 42 wherein the second semiconductor material comprises silicon and carbon.

45. The inverter of claim 26 wherein the semiconductor substrate further comprises an insulator layer underlying the first semiconductor material.

46. The inverter of claim 26 and further comprising a conductive material formed over the source region and the drain region.

47. The inverter of claim 46 wherein the conductive material at least one material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide, tantalum silicide, erbium silicide, iridium silicide, cobalt germanosilicide, nickel germanosilicide, cobalt carbon-silicide, nickel carbon-silicide.

48. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a semiconductor.

49. The inverter of claim 48 wherein the gate electrode is formed from polycrystalline silicon.

50. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal.

51. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal silicide.

52. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal nitride.

53. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, wherein the gate dielectric comprises at least one material selected from the group consisting of silicon oxide, silicon oxynitride, and silicon nitride.

54. The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, wherein the gate dielectric comprises a high k dielectric.

55. The inverter of claim 54 wherein the gate dielectric comprises at least one material selected from the group consisting of hafnium oxide, aluminum oxide, and zirconium oxide, and combinations thereof.

56. A method of forming a semiconductor structure, the method comprising:

providing a semiconductor substrate that includes a semiconductor body formed of a first semiconductor material;

defining a first active area and a second active area in the semiconductor body;

forming a first transistor in the first active area, the first transistor including a source region and a drain region formed in the semiconductor body oppositely adjacent a channel region, the first transistor further including a gate dielectric overlying the channel region and a first gate electrode overlying the first gate dielectric, wherein the first channel region is formed in the first semiconductor material and at least a portion of the source region and the drain region is formed in a second semiconductor material, the second semiconductor material having a lattice constant that is different than a lattice constant of the first semiconductor material;

forming a second element in the second active area; and

forming a conductor between the drain of the transistor and the load element.

57. The method of claim 56 wherein the second element comprises a second transistor including a conductivity type different than that of the first transistor, the second transistor having second source and drain regions in the substrate oppositely adjacent a second channel region, wherein the conductor is formed between the drain the first transistor and the drain of the second transistor.

58. The method of claim 57 and further comprising:

electrically coupling the source of the first transistor to a first supply voltage node; and

electrically coupling the source of the second transistor to a second supply voltage node.

59. The method of claim 56 wherein the second element comprises a resistor.

60. The method of claim 59 wherein the resistor comprises a first terminal and a second terminal such that the conductor is formed between the drain of the transistor and the first terminal of the resistor, the method further comprising:

electrically coupling the source of the first transistor to a first supply voltage node; and

electrically coupling the second terminal of the resistor to a second supply voltage node.

61. The method of claim 56 wherein forming a first transistor comprises:

forming a gate stack that includes the gate dielectric and the gate electrode;

forming a dielectric layer over the first active area including the gate stack;

anisotropically etching the dielectric layer to form sidewall spacers along sidewalls of the gate electrode;

etching a portion of the semiconductor body to form trenches adjacent the sidewall spacers; and

forming the second semiconductor material in the trenches.

62. The method of claim 61 and further comprising implanting dopants through the second semiconductor material and into the semiconductor body to form the source and drain regions.

63. The method of claim 62 wherein the source and drain regions extend at least 1000 angstroms into the semiconductor body.

64. The method of claim 63 wherein the second semiconductor material has thickness of less than about 200 angstroms.

65. The method of claim 61 and further comprising forming a layer of the first semiconductor material over the second semiconductor material.

66. The method of claim 61 wherein forming a gate stack further comprises forming a second gate stack over the second active area and wherein forming a dielectric layer comprises forming a dielectric layer over the first active area and the second active area.

67. The method of claim 66 and further comprising forming a mask over the second active area after forming the dielectric layer but before anisotropically etching.

68. The method of claim 56 wherein the lattice constant of the second semiconductor material is larger than the lattice constant of the first semiconductor material.

69. The method of claim 68 wherein the first transistor is a PMOS transistor.

70. The method of claim 69 wherein the second semiconductor material comprises silicon and germanium.

71. The method of claim 70 wherein the second semiconductor material comprises silicon, germanium, and carbon.

72. The method of claim 70 wherein the concentration of germanium is greater than 10 percent.

73. The method of claim 56 wherein the lattice constant of the second semiconductor material is smaller than the lattice constant of the first semiconductor material.

74. The method of claim 73 wherein the first transistor is an NMOS transistor.

75. The method of claim 74 wherein the second semiconductor material comprises silicon and carbon.

76. The method of claim 75 wherein the second semiconductor material comprises silicon, germanium, and carbon.

77. The method of claim 75 wherein the concentration of carbon is in the range of 0.01 percent to 0.04 percent.